



正基科技股份有限公司

SPECIFICATION

PRODUCT NAME : AP6398P

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正基科技股份有限公司



AP6398P Data Sheet

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Revision

Revision	Date	Description	Revised By
0.6	2019 / 11 / 19	- Revise Format	Jerry Wu
1.0	2020 / 12 / 08	- Official version	Richard
1.1	2022/ 06 / 17	-Update Bluetooth spec to 5.2	Jason
1.2	2024/ 12 / 19	-Update Bluetooth spec to 5.4	Ali

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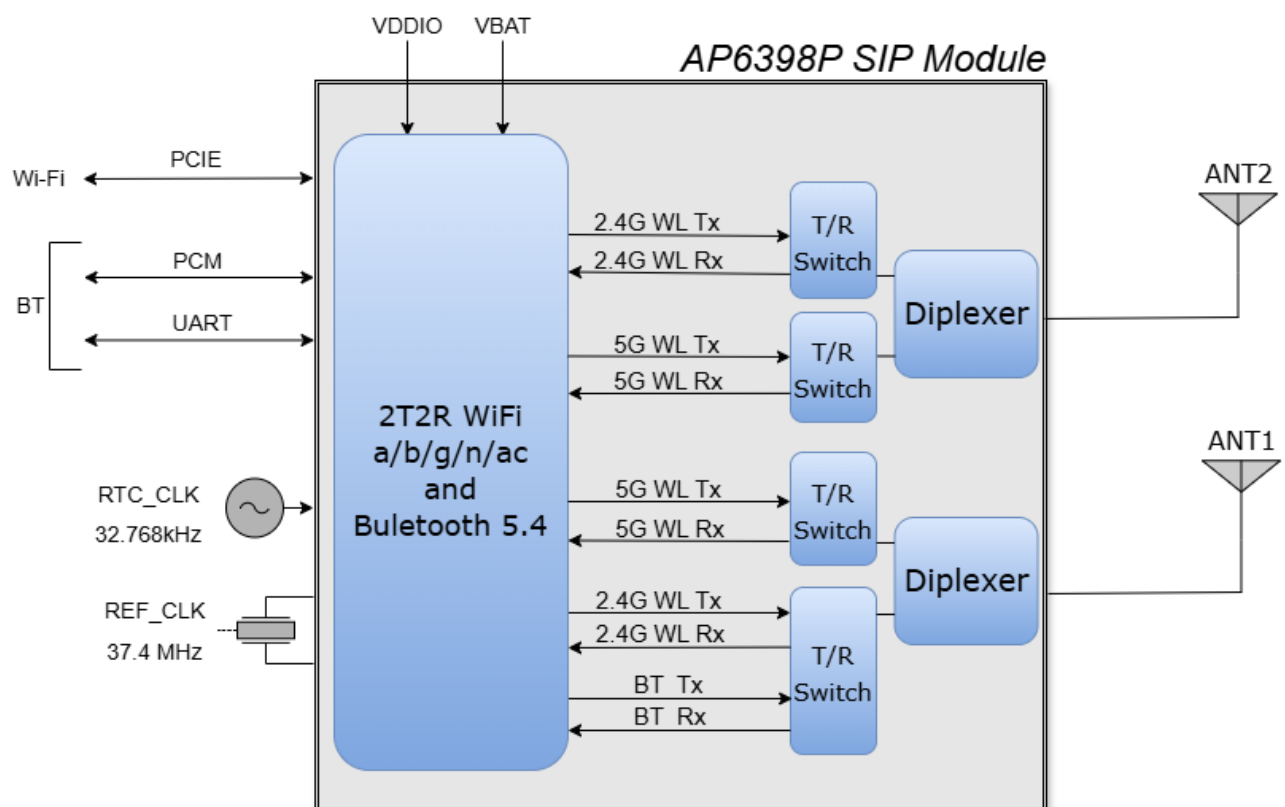
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1. Introduction

1.1 Overview

The AMPAK Technology® AP6398P is a fully Wi-Fi and Bluetooth functionalities module with seamless roaming capabilities and advance security, also it could interact with different vendors' 802.11a/b/g/n/ac 2x2 Access Points with MIMO standard and can accomplish up to speed of 866.7Mbps with single stream in 802.11ac to connect the wireless LAN. Furthermore AP6398P included PCI-E interface for Wi-Fi, UART/ PCM interface for Bluetooth.

In addition, this compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for tablet, OTT box and portable devices.



1.2 Product Features

- Lead Free design which is compliant with ROHS requirements.
 - TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
 - Dual-stream spatial multiplexing up to 866.7 Mbps data rate.
 - 20, 40, 80 MHz channels with optional SGI (256 QAM modulation)
 - Supports 1antenna with one for WLAN & Bluetooth shared port. Also, shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.
 - Supports PCIE 3.0 for x1 lane and power management running at Gen1 speeds.
 - BT host digital interface:
 - HCI UART (up to 4 Mbps)
 - PCM for audio data
 - Complies with Bluetooth Core Specification Version 5.4 with provisions for supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation.
 - Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
 - Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- A simplified block diagram of the module is depicted in the figure above.

2. General Specification

2.1 General Specification

Model Name	AP6398P
Product Description	2Tx/2Rx 802.11 ac/a/b/g/n Wi-Fi + Bluetooth 5.4 Module
Dimension	L x W: 15 x 13(Typ.)mm 、 H : 1.77 (Max.) mm
WiFi Interface	PCIE V3.0-compliant interface running at Gen1 speeds.
BT Interface	UART / PCM
Operating temperature	-30°C to 75°C
Storage temperature	-40°C to 125°C
Humidity	Operating Humidity : Less than 85% Non-Condensing

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10 °C to +55 °C and 3.2V < VBAT < 3.8V without derating performance.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	4.5	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.8	V

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage.

Symbol	Condition	Minimum ESD Rating	Unit
ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	1	kV
ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	250	V



2.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.0	3.3	3.8	V
VDDIO	1.7	1.8 / 3.3	3.6	V

VBAT current consumption 1.2A (Peak), when VBAT = 3.3V

The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	Min.	Max.	Unit
VIL/VIH	$0.35 \times \text{VDDIO}$	$0.65 \times \text{VDDIO}$	V
VOL/VOH output@2mA	0.45	VDDIO-0.45	V
For VDDIO=3.3V	Min.	Max.	Unit
VIL/VIH	0.80	2	V
VOL/VOH output@2mA	0.4	VDDIO-0.4	V

3. Wi-Fi RF Specification

3.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11b/g/n & Wi-Fi compliant			
Frequency Range		2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band)			
Number of Channels		2.4GHz : Ch1 ~ Ch13			
Modulation		802.11b : DQPSK 、DBPSK 、CCK 802.11 g/n : OFDM /64-QAM 、16-QAM 、QPSK 、BPSK			
Output Power , tolerance ± 1.5 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps	
	17.5	17.5	17.5	17.5	
802.11g	6 、 9Mbps	12 、 18Mbps	24Mbps	36Mbps	48Mbps
	17.5	17.5	17	17	16.5
	54Mbps				
	16.5				
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6
	17.5	16.5	16.5	16	16
	MCS7				
	15.5				
Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.					
Sensitivity, tolerance ± 2 dB					
CCK modulation PER ≤ 8% 、 OFDM modulation PER ≤ 10%					
802.11b	Data Rate	Spec.(dBm)			
	1Mbps	-96			
	2Mbps	-93			
	5.5Mbps	-91			
	11Mbps	-88			
802.11g SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)	
	6Mbps	-92	24Mbps	-84	
	9Mbps	-91	36Mbps	-81	

	12Mbps	-90	48Mbps	-78
	18Mbps	-87	54Mbps	-76
802.11g MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-95	24Mbps	-87
	9Mbps	-94	36Mbps	-84
	12Mbps	-93	48Mbps	-81
	18Mbps	-90	54Mbps	-78
802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-91	MCS4	-80
	MCS1	-89	MCS4	-78
	MCS2	-87	MCS6	-76
	MCS3	-78	MCS7	-74
802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-93	MCS5	-80
	MCS1	-92	MCS6	-78
	MCS2	-90	MCS7	-76
	MCS3	-87	MCS8	-92
	MCS4	-83	MCS15	-73
Maximum Input Level	802.11b : -10 dBm			
	802.11g/n : -20 dBm			

3.2 5GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11a/n/ac & Wi-Fi compliant			
Frequency Range		5.15~5.35GHz 、 5.47~5.725GHz 、 5.725~5.85GHz (5GHz UNII Band)			
Number of Channels		5.15~5.35GHz ： Ch36 ~ Ch64 5.47~5.725GHz ： Ch100 ~ Ch140 5.725~5.85GHz ： Ch149 ~ Ch165			
Modulation		802.11a ： OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11n ： OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ac ： OFDM /256-QAM 、 OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK			
Output Power , tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11a	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5150~5350	16.5	16.5	16	16
	5470~5720	16.5	16.5	16	16
	5725~5845	16.5	16.5	16	16
	Frequency (MHz)	48Mbps	54Mbps		
	5150~5350	15.5	15.5		
	5470~5720	15.5	15.5		
	5725~5845	15.5	15.5		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	15.5	15.5
	5470~5720	16	16	15.5	15.5
	5725~5845	16	16	15.5	15.5
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	14.5	14.5		
	5470~5720	14.5	14.5		
	5725~5845	14.5	14.5		
802.11n 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	15.5	15.5
	5470~5720	16	16	15.5	15.5
	5725~5845	16	16	15.5	15.5
	Frequency (MHz)	MCS6	MCS7		

	5150~5350	14.5	14.5		
	5470~5720	14.5	14.5		
	5725~5845	14.5	14.5		
802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	15.5	15.5
	5470~5720	16	16	15.5	15.5
	5725~5845	16	16	15.5	15.5
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5350	14.5	14.5	12	
	5470~5720	14.5	14.5	12	
	5725~5845	14.5	14.5	12	
802.11ac 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	15.5	15.5
	5470~5720	16	16	15.5	15.5
	5725~5845	16	16	15.5	15.5
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	14.5	14.5	12	10
	5470~5720	14.5	14.5	12	10
	5725~5845	14.5	14.5	12	10
802.11ac 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15	15	14	14
	5470~5720	15	15	14	14
	5725~5845	15	15	14	14
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	13	13	12	10
	5470~5720	13	13	12	10
	5725~5845	13	13	12	10

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB

CCK modulation PER $\leq 8\%$ 、OFDM modulation PER $\leq 10\%$

802.11a SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-91	24Mbps	-83
	9Mbps	-90	36Mbps	-80
	12Mbps	-88	48Mbps	-76
	18Mbps	-86	54Mbps	-74

802.11a MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-92	24Mbps	-86
	9Mbps	-91	36Mbps	-83
	12Mbps	-90	48Mbps	-78
	18Mbps	-89	54Mbps	-77

802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS4	-79
	MCS1	-88	MCS5	-76
	MCS2	-86	MCS6	-73
	MCS3	-83	MCS7	-72
802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-92	MCS5	-78
	MCS1	-91	MCS6	-76
	MCS2	-89	MCS7	-75
	MCS3	-86	MCS8	-89
	MCS4	-82	MCS15	-70
802.11n_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS4	-77
	MCS1	-86	MCS5	-72
	MCS2	-83	MCS6	-70
	MCS3	-80	MCS7	-69
802.11n_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-75
	MCS1	-88	MCS6	-73
	MCS2	-86	MCS7	-72
	MCS3	-83	MCS8	-86
	MCS4	-79	MCS15	-67
802.11ac_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS5	-75
	MCS1	-88	MCS6	-73
	MCS2	-86	MCS7	-70
	MCS3	-83	MCS8	-67
	MCS4	-79		
802.11ac_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)

MIMO	MCS0,NSS=1	-92	MCS6,NSS=1	-76
	MCS1,NSS=1	-91	MCS7,NSS=1	-75
	MCS2,NSS=1	-88	MCS8,NSS=1	-72
	MCS3,NSS=1	-85	MCS0,NSS=2	-88
	MCS4,NSS=1	-82	MCS8,NSS=2	-65
	MCS5,NSS=1	-77		
802.11ac_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-72
	MCS1	-86	MCS6	-70
	MCS2	-83	MCS7	-69
	MCS3	-80	MCS8	-65
	MCS4	-76	MCS9	-63
802.11ac_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-90	MCS6,NSS=1	-73
	MCS1,NSS=1	-88	MCS7,NSS=1	-72
	MCS2,NSS=1	-86	MCS8,NSS=1	-68
	MCS3,NSS=1	-82	MCS9,NSS=1	-66
	MCS4,NSS=1	-79	MCS0,NSS=2	-86
	MCS5,NSS=1	-77	MCS9,NSS=2	-60
802.11ac_80MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-85	MCS5	-68
	MCS1	-82	MCS6	-67
	MCS2	-79	MCS7	-65
	MCS3	-76	MCS8	-62
	MCS4	-73	MCS9	-60
802.11ac_80MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-87	MCS6,NSS=1	-70
	MCS1,NSS=1	-85	MCS7,NSS=1	-68
	MCS2,NSS=1	-82	MCS8,NSS=1	-66
	MCS3,NSS=1	-79	MCS9,NSS=1	-63
	MCS4,NSS=1	-76	MCS0,NSS=2	-83
	MCS5,NSS=1	-71	MCS9,NSS=2	-58
Maximum Input Level	802.11a/n/ac : -30 dBm			

4. Bluetooth Specification

4.1 Bluetooth Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

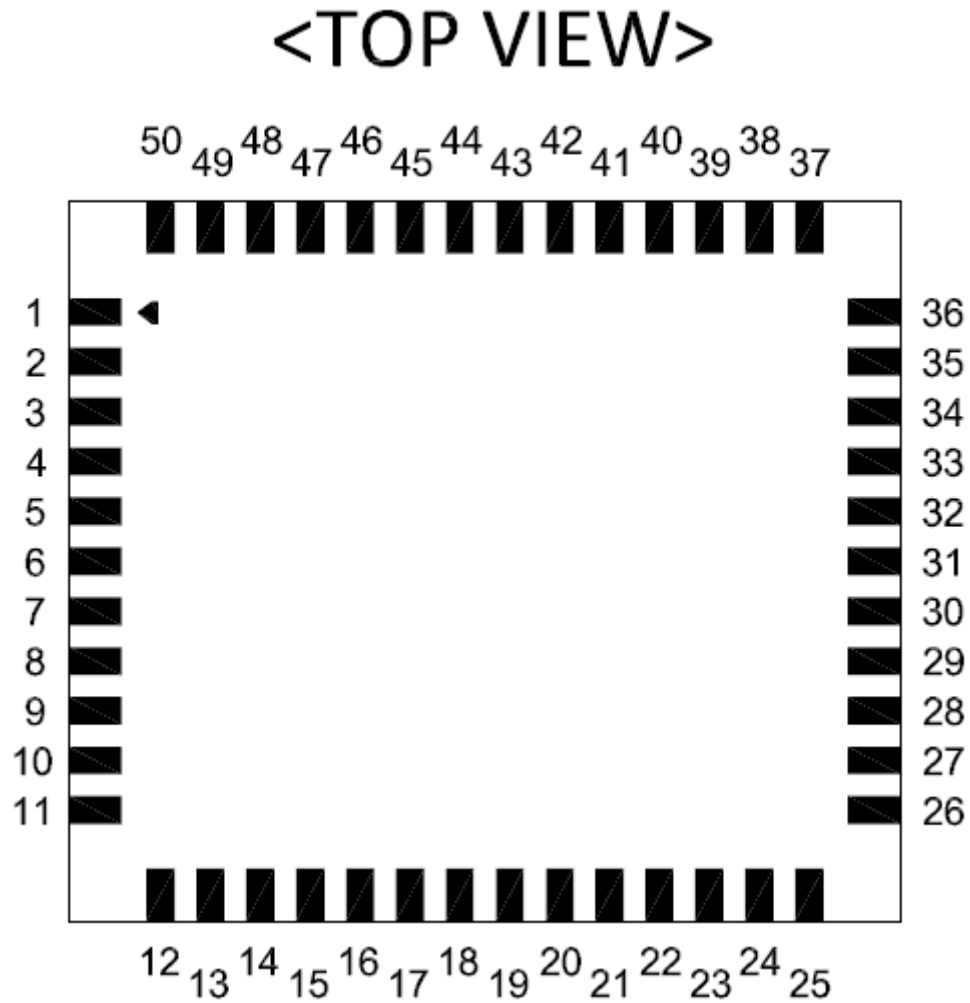
Feature	Description	
General Specification		
Bluetooth Standard	BDR 、EDR(2Mbps & 3Mbps) 、LE(1Mbps) 、2LE(2Mbps)	
Host Interface	UART	
Frequency Band	2402 MHz ~ 2480 MHz	
Number of Channels	79 channels for classic 、40 channels for BLE	
Modulation	GFSK, $\pi/4$ -DQPSK, 8DPSK	
RF Specification		
Output Power , tolerance ± 2 dB		
	CL1 (dBm)	CL2 (dBm)
BDR Output Power	6.5	2
EDR Output Power	5.5	2
LE Output Power	5.5	2
Sensitivity, tolerance ± 1.5 dB		
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-86dBm	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)	-88dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-84dBm	
Sensitivity @ PER=30.8% for LE (1Mbps)	-89dBm	
Sensitivity @ PER=30.8% for LE (2Mbps)	-90dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm	
	$\pi/4$ -DQPSK (2Mbps) :-20dBm	
	8DPSK (3Mbps) :-20dBm	

Note* : The Bluetooth output power is able to be configured by firmware (hcd file).



5. Pin Definition

5.1 Pin Outline



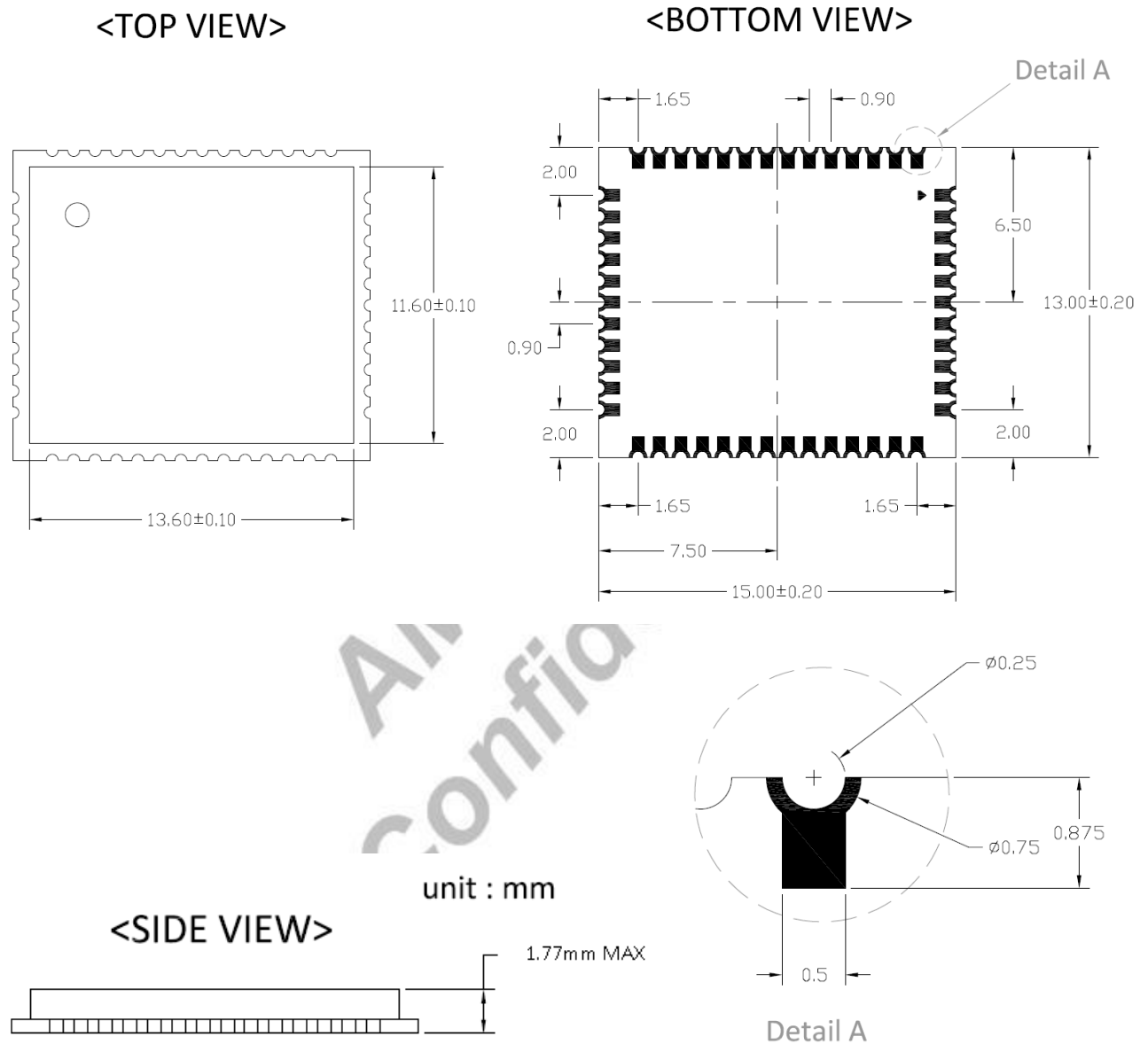
5.2 Pin Assignment

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL/BT_ANT0	I/O	RF I/O port0
3	GND	—	Ground connections
4	GND	—	Ground connections
5	GND	—	Ground connections
6	GND	—	Ground connections
7	GND	—	Ground connections
8	GND	—	Ground connections
9	WL_ANT1	I/O	RF I/O port1
10	GND	—	Ground connections
11	GND	—	Ground connections
12	PCIE_PREST_L	I	PCIe host indication to reset the device
13	XTAL_OUT	O	External Crystal out
14	XTAL_IN	I	External Crystal in/ Single clock source in
15	WL_REG_ON	I	Low asserting reset for WiFi core
16	WL_HOST_WAKE	O	WLAN to wake-up HOST
17	NC	—	No connect
18	NC	—	No connect
19	NC	—	No connect
20	NC	—	No connect
21	NC	—	No connect
22	NC	—	No connect
23	GND	—	Ground connections
24	PCIE_PME_L	OD	PCI power management event output
25	VIN_LDO	P	Internal Buck voltage generation pin
26	VIN_LDO_OUT	P	Internal Buck voltage generation pin
27	PCM_SYNC	I/O	PCM sync signal
28	PCM_IN	I	PCM data input
29	PCM_OUT	O	PCM Data output
30	PCM_CLK	I/O	PCM clock
31	LPO	I	External Low Power Clock input (32.768KHz)
32	GND	—	Ground connections

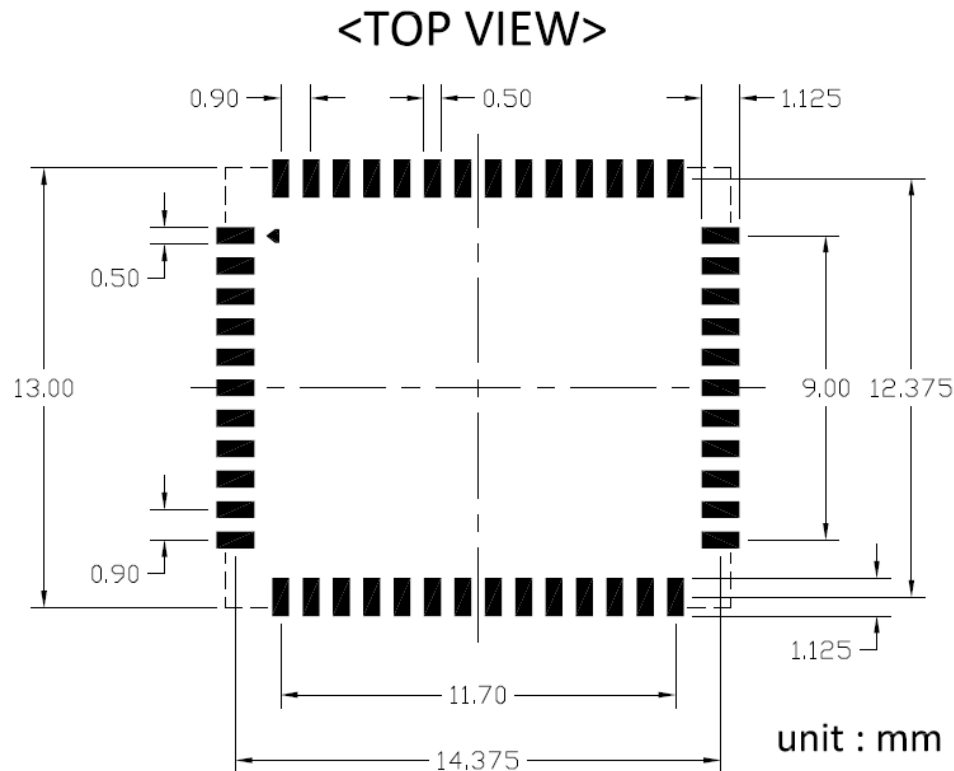
33	PCIE_RCLK_N	I	PCI Express differential clock input-Negative
34	VDDIO	P	I/O Voltage supply input
35	PCIE_RCLK_P	I	PCI Express differential clock input-Positive
36	VBAT	P	Main power voltage source input
37	PCIE_CLKREQn	OD	PCIe clock request
38	BT_REG_ON	I	Low asserting reset for Bluetooth core
39	GND	—	Ground connections
40	UART_TXD	O	Bluetooth UART interface
41	UART_RXD	I	Bluetooth UART interface
42	UART_RTS_N	O	Bluetooth UART interface
43	UART_CTS_N	I	Bluetooth UART interface
44	PCIE_RX_N	I	PCI Express receive data-Negative
45	PCIE_RX_P	I	PCI Express receive data-Positive
46	PCIE_TX_N	O	PCI Express transmit data-Negative
47	PCIE_TX_P	O	PCI Express transmit data-Positive
48	NC	—	No connect
49	BT_WAKE	I	HOST wake-up Bluetooth device
50	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST

6. Dimensions

6.1 Module Dimensions

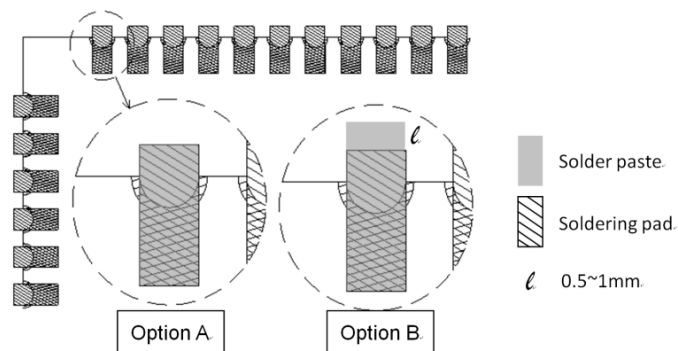


6.2 Recommended Footprint



- Solder paste layer design is generally the same as recommended footprint.
(錫膏層設計通常建議和焊墊尺寸相同)
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial. In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact AMPAK FAE for assistance.

(如果模組吃錫品質考量側面爬錫，如何優化鋼網開孔設計以調整適當的錫膏量是非常重要的。尤其鋼網的厚度大約是 0.1mm 或更薄時，可考慮局部加厚鋼網的設計。請諮詢製程工程師以優化鋼網的設計,或是聯絡正基科技技術支持團隊)。



7. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V _{io} - V _{io}	V

Input signal amplitude follow VDDIO (1.8V or 3.3V)

External 37.4MHz X'TAL characteristics

Parameter	Specification	Units
Nominal frequency - F ₀	37.4	MHz
Frequency Tolerance - $\Delta F / F_0$ (At 25°C +/- 3°C)	+/- 5	ppm
Operation Temperature Range - Topr	-30 ~ + 85	°C
Freq. Stability(over operating temperature) - TC Ref. to 25°C	+/- 15	ppm
Load capacitance - CL	16	pF
Equivalent Series Resistance – ESR	Max. 60	Ω
Drive Level - DL	Typ. 50, Max. 100	μ W
Insulation resistance – IR At 100Vdc	Min. 500	M Ω

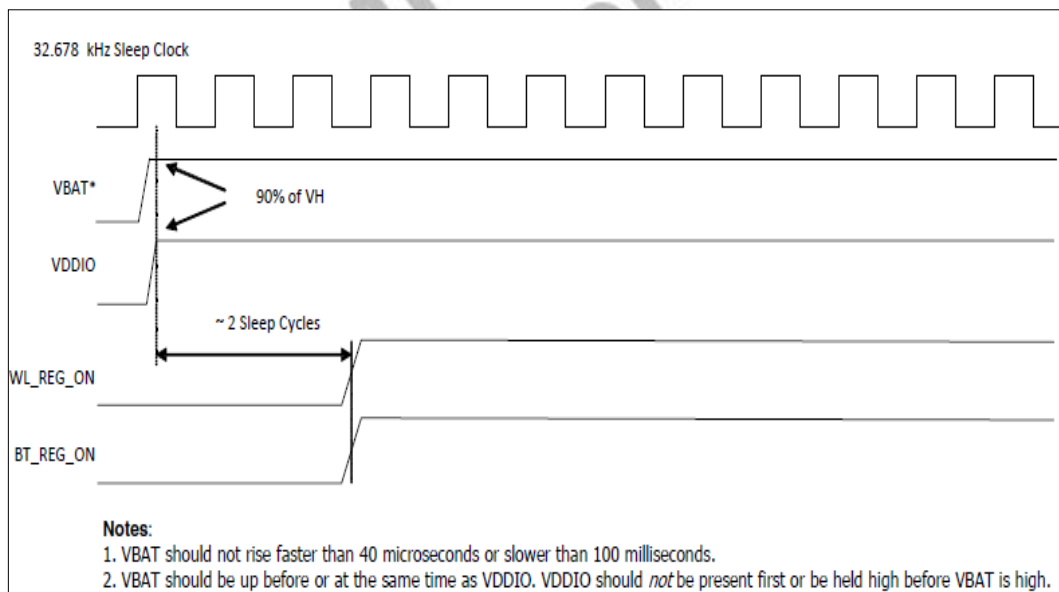
8. Host Interface Timing Diagram

8.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

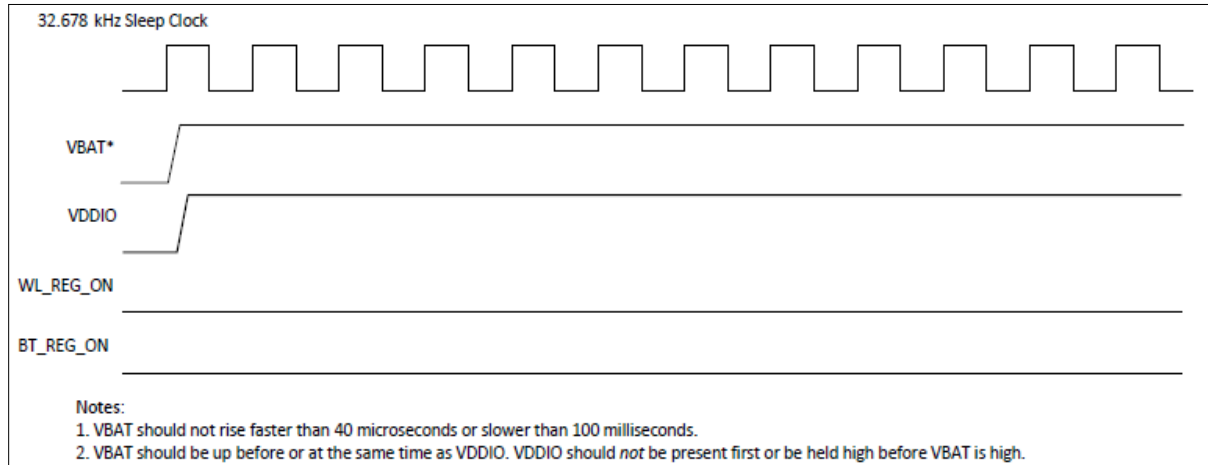
Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

- **WL_REG_ON**: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- **BT_REG_ON**: Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).

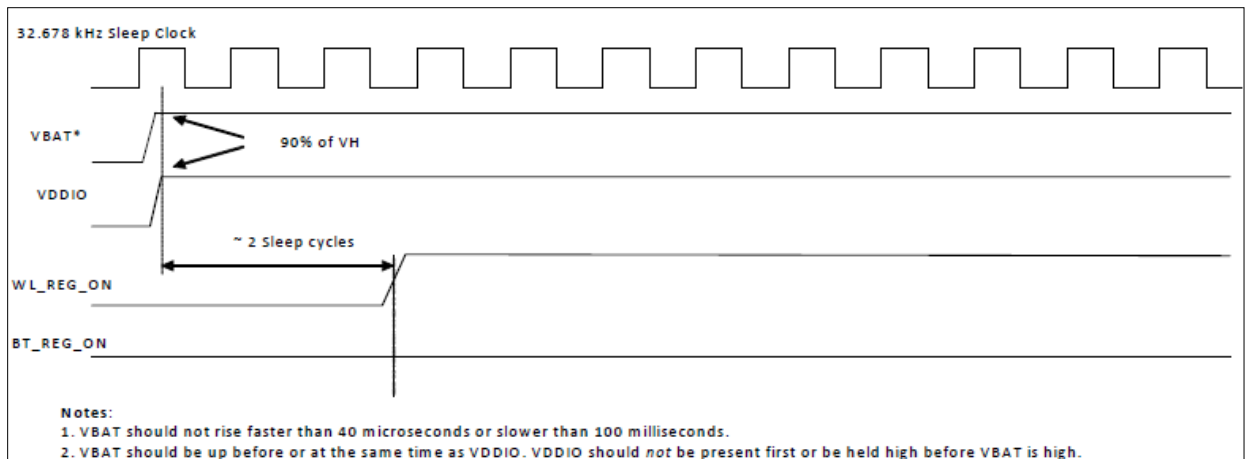


WLAN=ON, Bluetooth=ON

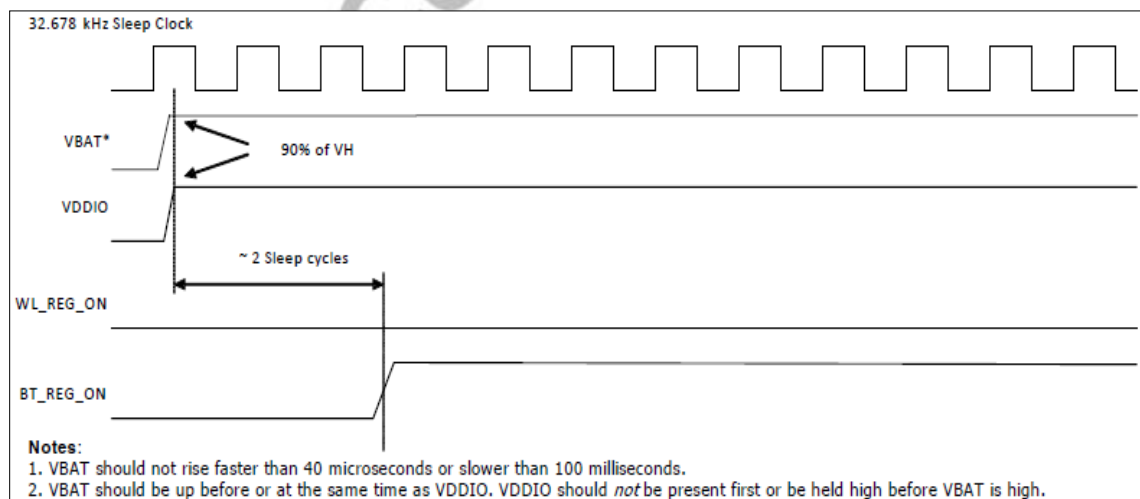




WLAN=OFF, Bluetooth=OFF



WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

8.2 PCI-E Power -up

Timing Parameter WL_REG_ON (Pers# Deassertion-First Config Access)

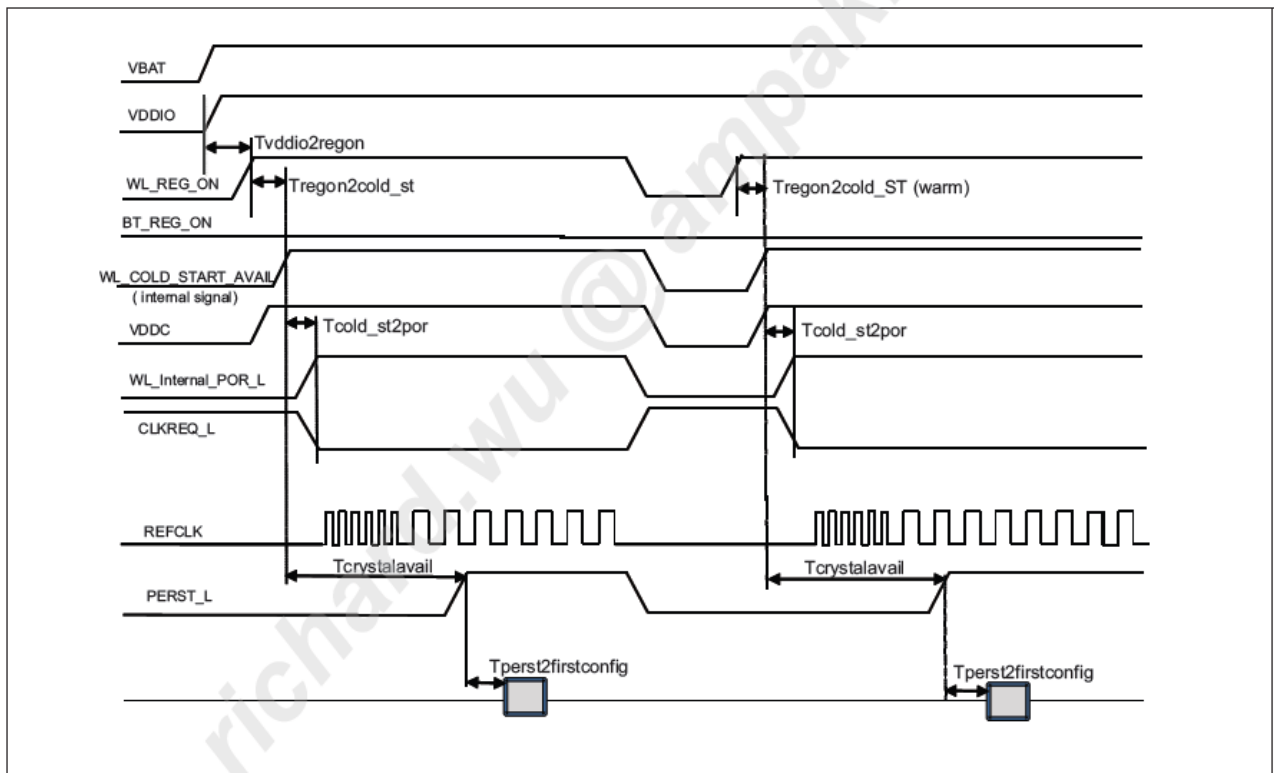
Timing Parameter	Value	Unit
Tvddio2regon	0.1	ms
Tregon2cold_st (3.4 ms + 162 ILP cycles)	10.13	ms
Tcold_st2por (54 ILP cycles)	2.24	ms
Tcrystalavail (509 ILP cycles)	21.17	ms
Tperst2firstconfig	6.00	ms
Tvddioon2firstconfig (Tvddio2regon + Tregon2cold_st + Tcrystalavail + Tperst2firstconfig)	37.4	ms
Tregonwcold_st (warm) (162 ILP cycles)	6.73	ms

Tvddioon2firstconfig: Taking VDDIO as reference, 37.4 ms is the minimum time that a system must wait before issuing first config access.



Note: Take internal ILP with $\pm 30\%$ tolerance for the above calculations.

PCIe Power-On Timing

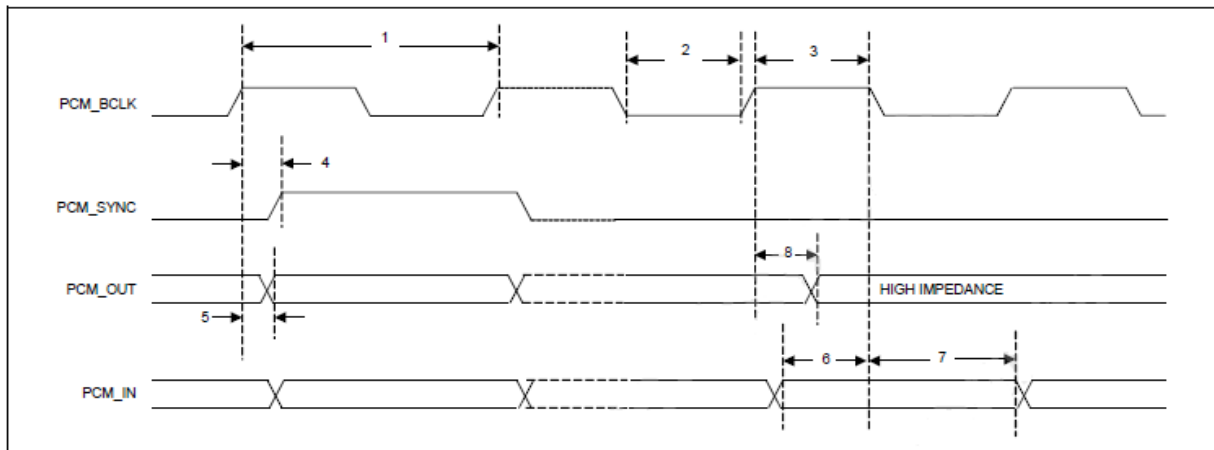


8.3 PCM Interface Description

The PCM Interface on the AP6398P can connect to linear PCM Codec devices in master or slave mode. In master mode, the AP6398P generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the AP6398P. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Short Frame Sync, Master Modem

PCM Timing Diagram (Short Frame Sync, Master Mode)



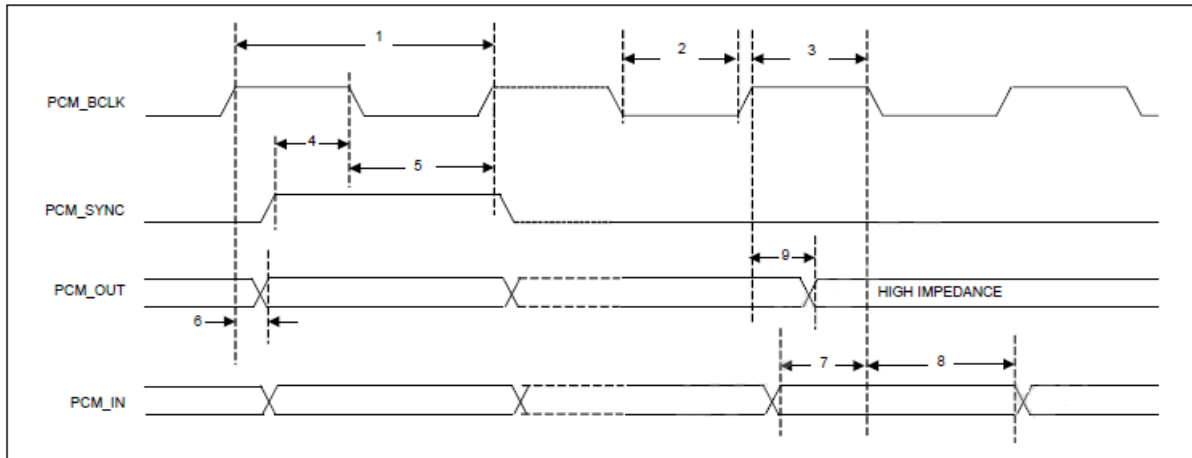
PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns



Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)



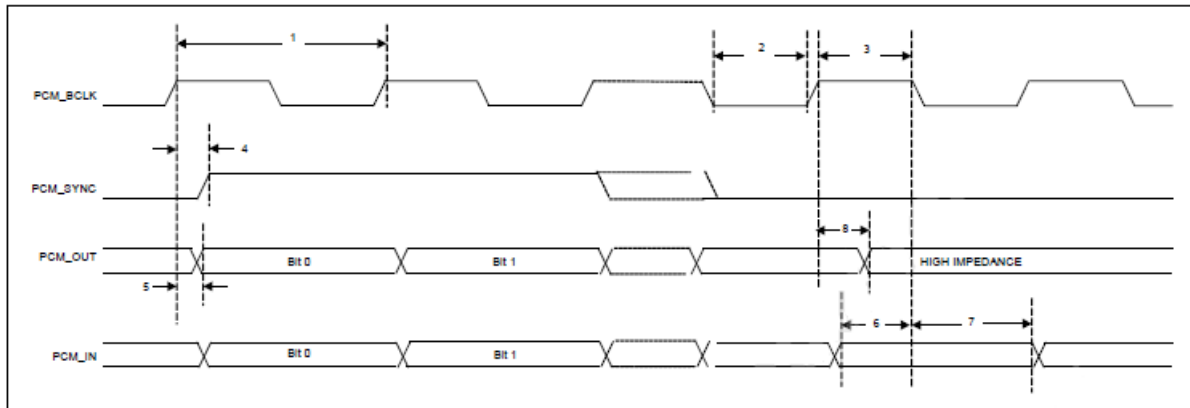
PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns



Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)



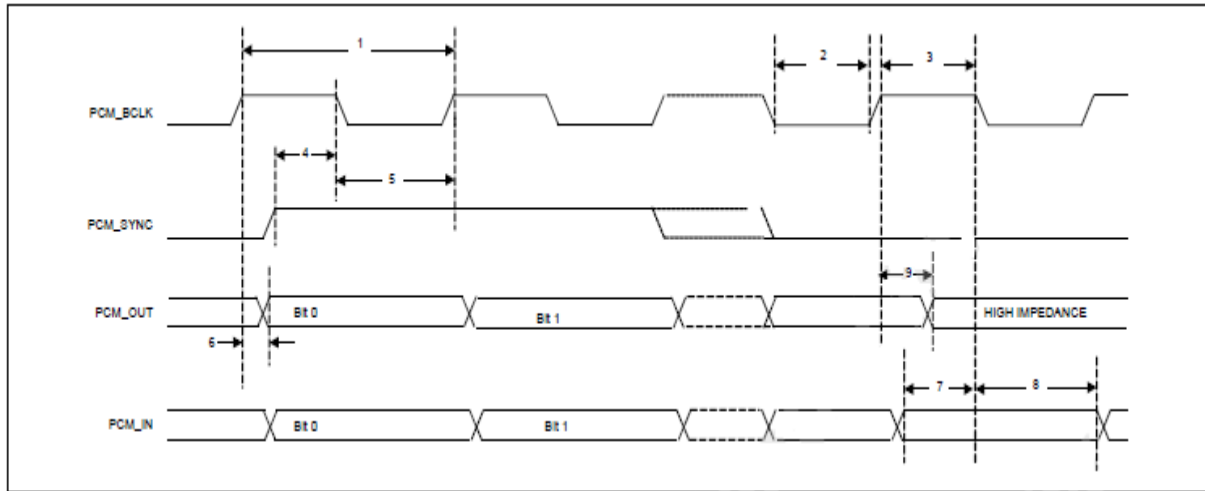
PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns



Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)



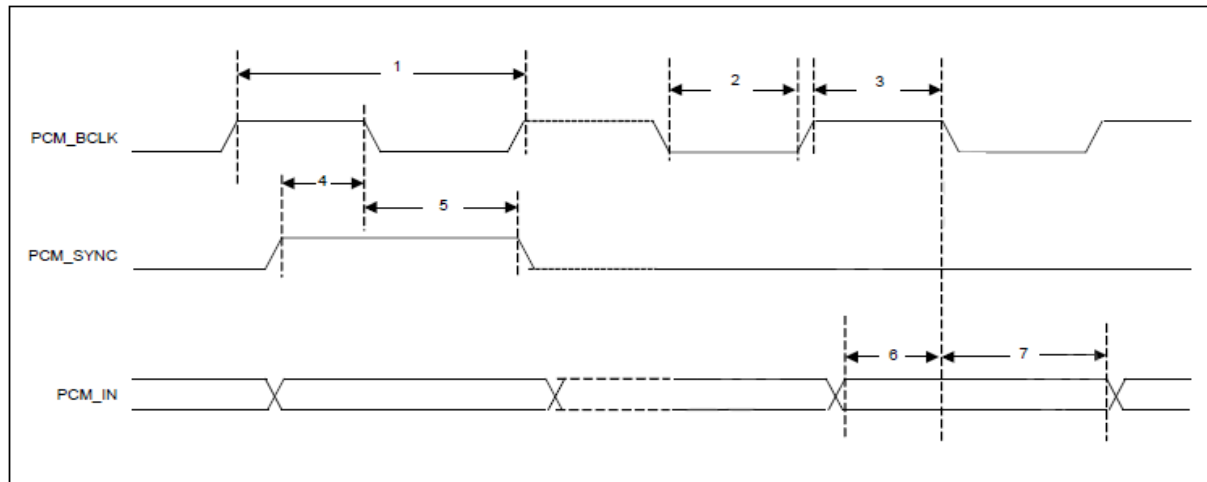
PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns



Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)



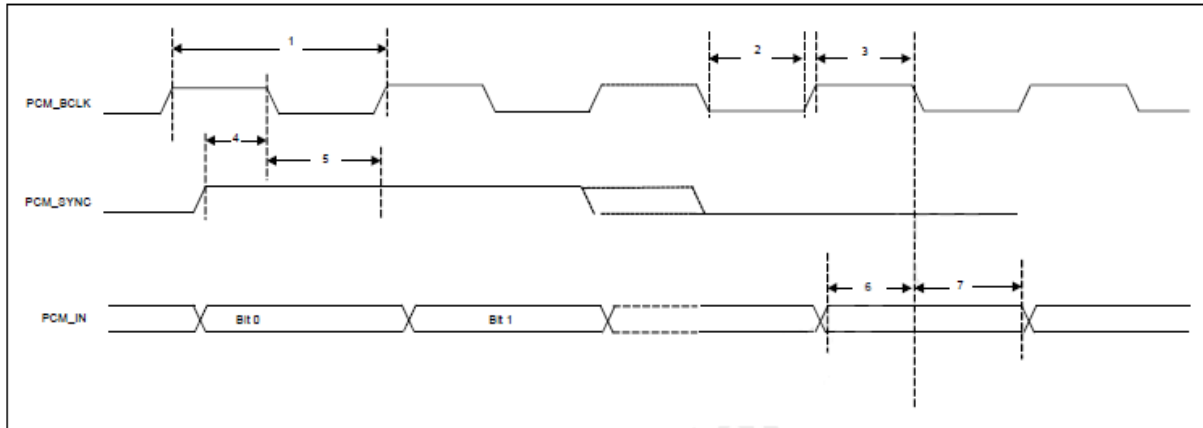
PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns



Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)



PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns



8.4 UART Interface Description

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.4 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The AP6398P UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

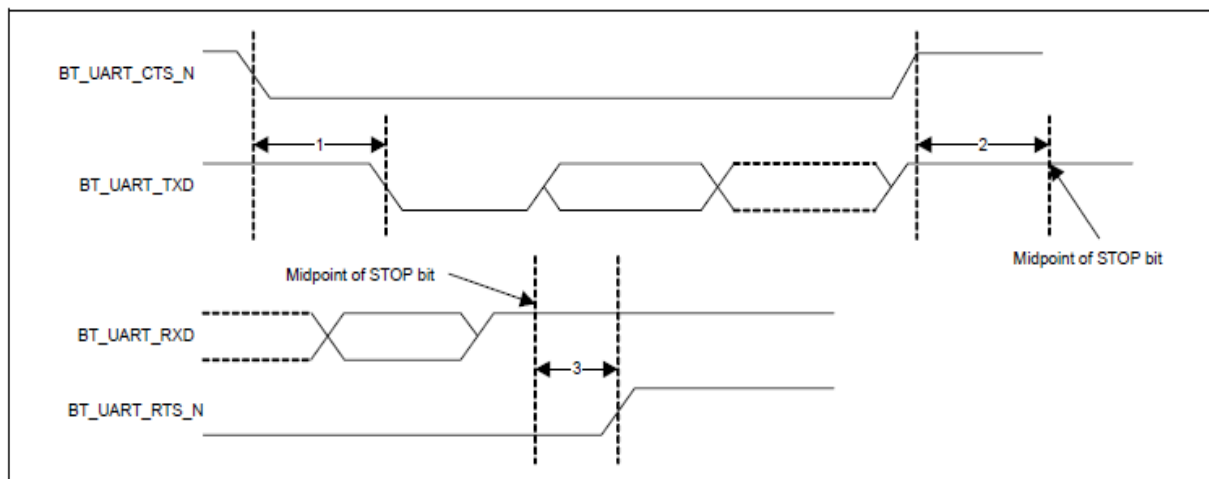
Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AP6398P UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within $\pm 2\%$.



Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

UART Timing

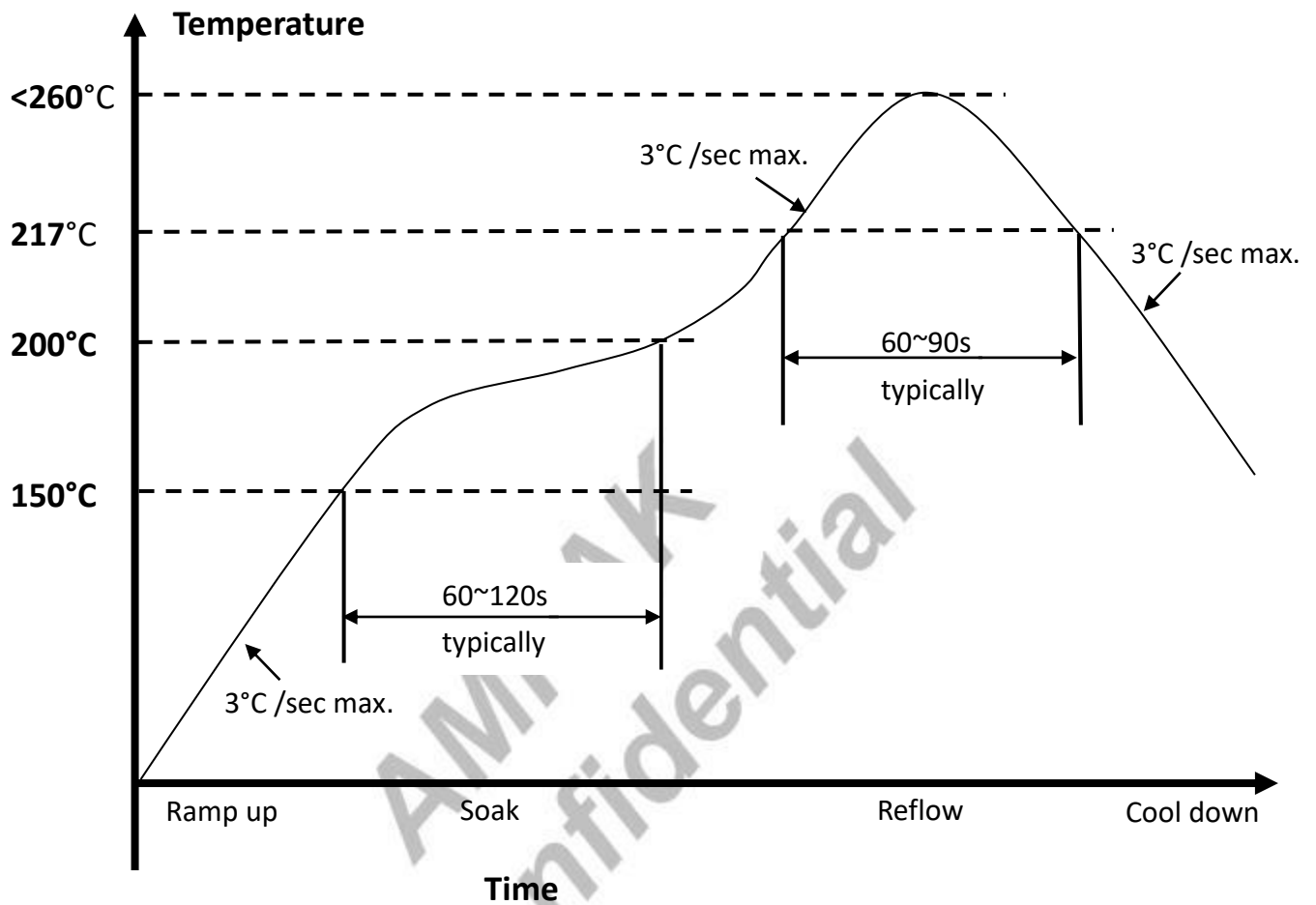


UART Timing Specifications

Ref	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods



9. Recommended Reflow Profile



1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C
3. Cycle of Reflow : 2 times max.
4. Adding Nitrogen (N₂) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component.

10. Package Information

10.1 Label

Label A → Anti-static and humidity notice



Label B → MSL caution / Storage Condition

Caution		LEVEL
This bag contains MOISTURE-SENSITIVE DEVICES		☐ If blank, see adjacent bar code label
1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH) 2. Peak package body temperature: _____ °C If blank, see adjacent bar code label 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be a) Mounted within: _____ hours of factory conditions If blank, see adjacent bar code label ≤30°C/60% RH, or b) Stored per J-STD-033 4. Devices require bake, before mounting, if: a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C b) 3a or 3b are not met 5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure Bag Seal Date: _____ If blank, see adjacent bar code label Note: Level and body temperature defined by IPC/JEDEC J-STD-020		

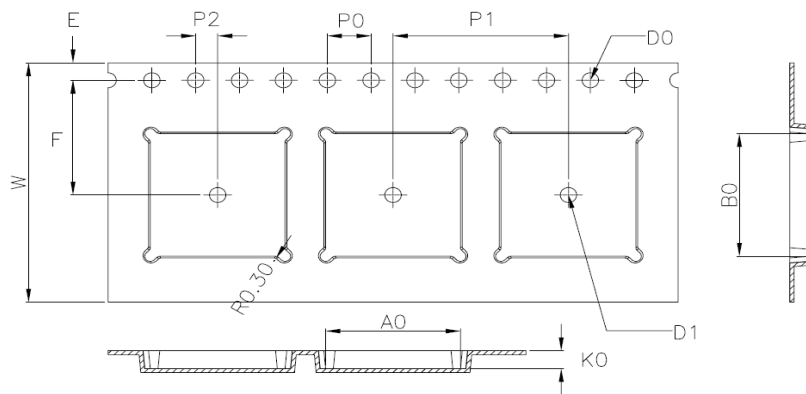
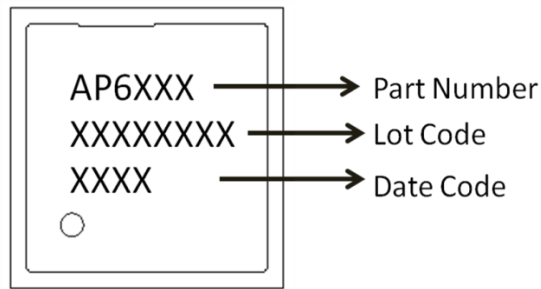
Label C → Inner box label .

PO:	
AMK DEVICE:	
PKG S/N:	 9PKGYYMDDNNNNN
Model Name:	 APXXXXXXXX (R3HF)
P/N:	 99X-XXX-XXXXR
Quantity:	 XXXX
Date Code:	 YYWW
Lot Code:	 XXXXXXXX

Label D → Carton box label .

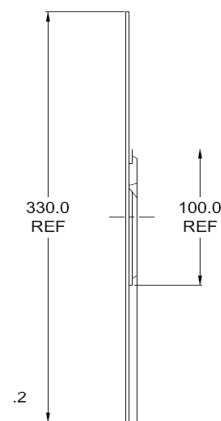
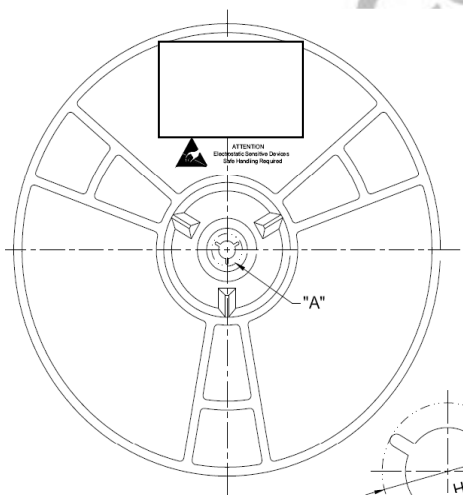
AMPAK Technology Inc.	
PO:	
AMK DEVICE:	
Model Name:	 APXXXXXXXX (R3HF)
Part No.:	 99X-XXX-XXXXR
Quantity:	 XXXX
Lot D/C:	 XXXXXXXX YYWW XXXX
Manufacture:	 YYYY/MM/DD

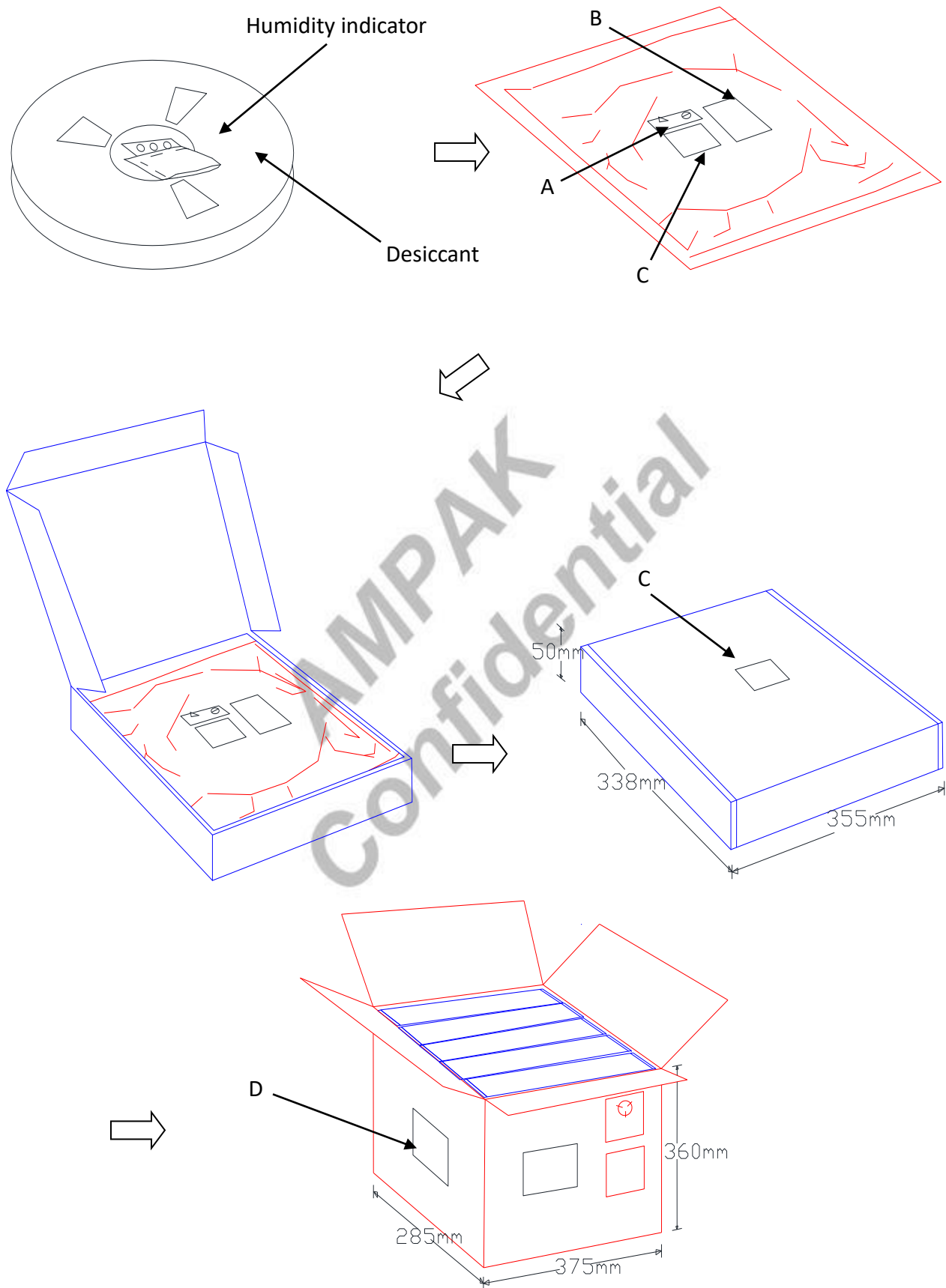
10.2 Dimension



W	24.00±0.30
A0	15.30±0.10
B0	13.30±0.10
K0	2.00±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	20.00±0.10
P2	2.00±0.10
D0	1.50 ^{+0.10} / _{-0.00}
D1	∅1.50MIN

1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material: Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness: 0.30±0.05mm.
6. Component load per 13" reel : 1000 PCS





10.3 MSL Level / Storage Condition

	Caution This bag contains MOISTURE-SENSITIVE DEVICES	LEVEL 4
If blank, see adjacent bar code label		
1. Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH)		
2. Peak package body temperature: <u>250</u> $^{\circ}\text{C}$ If blank, see adjacent bar code label		
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be		
a) Mounted within: <u>72</u> hours of factory conditions If blank, see adjacent bar code label		
$\leq 30^{\circ}\text{C}/60\% \text{ RH}$, or		
b) Stored per J-STD-033		
4. Devices require bake, before mounting, if:		
a) Humidity Indicator Card reads $>10\%$ for level 2a-5a devices or $>60\%$ for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$		
b) 3a or 3b are not met.		
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.		
Bag Seal Date: _____ If blank, see adjacent bar code label		
Note: Level and body temperature defined by IPC/JEDEC J-STD-020		